SYLLABUS

Name: ***Computer Architecture (MakAu>SI7CA19)***
Name in Polish:
Name in English: ***Computer Architecture***

Information on course:

Course offered by department: Faculty of Automatic Control, Electronics and Computer Science
Course for department: Silesian University of Technology

Default type of course examination report:

ZAL

Language:

English

Course homepage:

https://platforma.polsl.pl/rau2/course/view.php?id=218

Short description:

The aim of the lecture (semester 7) is to familiarize students with current solutions in the architecture and organization of processors, and then computer systems. Particular attention is paid to the mechanisms of parallelism in computer organization, distinguishing between instruction-level, data-level, and task-level parallelism. The lecture covers CISC and RISC processors, superscalar processors, graphics processors, multiprocessor systems with shared memory (servers), and computer clusters. Prerequisites: elementary knowledge, acquired in the Theory of Computer Science course, knowledge of the structure and role of basic components of computer systems: the control system, the arithmetic-logical unit, memory module, input/output devices, and instruction set. Students should have basic computer programming skills. The aim of the laboratory (semester 7) is to provide students with practical experience with various computer architectures and parallel and distributed programming tools

Description:

ECTS: 3
Total workload: 80 hours (60 contact hours, 20 hours of student work)
Contact hours:
Lecture 30 hours
Laboratory 30 hours
Student work: preparation for classes, preparation for the final test.

Lecture:
1) History of computer development
2) CISC, RISC, and RISC-V processor architectures
3) Instruction-level parallelism mechanisms - pipelined instruction execution, data hazard, and control hazard
4) Superscalar architecture - non-sequential instruction execution, new types of hazard, register renaming, dynamic instruction scheduling, instruction committing, branch prediction in superscalar processors - static and dynamic strategies, branch history-based predictors, neural branch predictors.
5) Hardware multithreading control in superscalar processors - fine-grained, coarse-grained, and simultaneous multithreading.
6) Examples of selected Intel and IBM processor architectures. ARM architecture.
7) VLIW architecture.
8) Parallelism models in processor architecture: Flynn's classification - SISD, SIMD, MIMD.
9) Processor architectures using data-level parallelism - historical vector and matrix processors, SIMD extensions for superscalar processors, GPU graphics processors - CUDA architecture, thread execution, SIMT model, GPU application for modeling neural networks - tensor cores.
10) Multiprocessor systems with shared memory - multicore processors, network topologies connecting cores, methods for checking core cache coherency, servers - characteristics, examples of available servers .
11) Multiprocessor systems with distributed memory – computer clusters, cluster characteristics, cluster organization models: Beowulf clusters, rack and blade clusters – examples, topologies and technologies of networks connecting cluster nodes, high-reliability cluster organization.
12) Massively parallel systems – supercomputers, the Top500 classification, examples of the largest supercomputers.
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Bibliography:

- A. Tanenbaum „Structured Computer Organization 6-th edition”, Pearson 2013.
- W. Stallings „Computer organization and architecture”, Pearson 2016.
John L. Hennessy, David A. Patterson „Computer Architecture: A Quantitative Approach”, Elsevier 2019.

-S. Kozielski „Architektura procesorów. Mechanizmy równoległości obliczeń – równoległość poziomu rozkazów” – Wydawnictwo Politechniki Śląskiej, 2024.
https://repolis.bg.polsl.pl/dlibra/publication/90432

Learning outcomes:

After attending the lectures, the student:
knows the architecture and organization of modern CISC, RISC, ARM, and superscalar processors (final test) - K1A_W10;
knows the details of the operation of commonly used superscalar processors and graphics processors (final test) - K1A_W10;
knows the architecture and organization of modern multiprocessor systems with shared memory (servers) and distributed memory (clusters) (final test) - K1A_W10, K1A_W14, K1A_U13, K1A_U25;
knows the development trends of specific computer architectures (final test) - K1A_W13;
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Assessment methods and assessment criteria:

The Computer Architecture course comprises two parts: lecture and laboratory. According to the study regulations, attendance at lectures is optional (but highly recommended), while participation in laboratory exercises is mandatory.

Lectures (semester 5) are assessed on the basis of a multiple-choice test; students must obtain at least half of the possible points.

The syllabus is effective from the summer semester of the 2025/2026 academic year, and its content can not change during the semester.
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Course credits in various terms:

<without a specific program>

Type of credits	Number	First term	Last term
European Credit Transfer System (ECTS)	3	2022/2023-Z	