SYLLABUS

Name: ***Design for testability (MSCKAu>SM21DFT22)***
Name in Polish:
Name in English: ***Design for testability***

Information on course:

Course offered by department: Faculty of Automatic Control, Electronics and Computer Science
Course for department: Silesian University of Technology

Default type of course examination report:

ZAL

Language:

English

Course homepage:

https://platforma2.polsl.pl/rau3/course/view.php?id=410

Short description:

The main objective of the course is to present the basic concepts related to digital circuits testing and their design for testability. The task of the course is also to familiarize students in practice with the basic techniques of testing digital circuits as well as the fundamental design methods that facilitate their testing.

The course participant should have a background in the theory of logic circuits, digital circuits design and hardware description languages

Description:

Syllabus description:

Lectures:
* Basic concepts regarding testing of digital circuits
* Basic fault types and fault modeling
* Testing philosophy, role of testing, process of testing digital circuits
* Economic aspects of testing and the impact of testing on product quality
* Test pattern generation for combinational and sequential circuits
* Testing connection networks

Design for testability solutions:
* Scan design
* Boundary scan (JTAG) and some related DFT standards
* Built-In Self-Test
* System level testing
* Fundamental ideas of reliability and fault tolerance

Laboratory:
* Test pattern generation for digital circuits
* Digital circuits testing with use of a boundary scan path
* Implementation of built-in self-test structures in digital circuits
* Introduction to designing fault-tolerant digital circuits

Total workload required to achieve learning outcomes:

Number of ECTS credits: 3
Total number of hours: 75 (40 contact hours / 35 student’s own work hours)
Contact hours:
* Lecture: 15h
* Laboratory classes: 15h
* Discussion of reports: 10h

Student workload hours:
* Reviewing the literature: 15h
* Preparation for the laboratory, preparation of reports: 20h

Number of ECTS credits allocated for contact hours: 1.6
Number of ECTS credits allocated for in-practice hours (laboratory classes, projects): 0.6

Bibliography:

Primary sources:

Samiha Mourad, Yervant Zorian: “Principles of Testing Electronic Systems”, John Wiley & Sons Inc., 2000

Bushnell M., Agrawal V. D.: “Essentials of Electronic Testing for Digital, Memory and Mixed-Signal VLSI Circuits”, Kluwer Academic Publishers, 2002

Charles E. Stroud: “A Designer's Guide to Built-in Self-Test”, Kluwer Academic Publishers, 2002

Secondary sources:

IEEE Std. 1149.1-2013, “IEEE Standard Test Access Port and Boundary-Scan Architecture”, IEEE, 2013

Parker K. P.: “The Boundary-Scan Handbook, 3rd Edition”, Kluwer Academic Publishers, 2003

Laung-Terng Wang, et al.: “VLSI Test Principles and Architectures: Design for Testability (The Morgan Kaufmann Series In Systems On Silicon)”, Morgan Kaufmann, 2006

Hławiczka A. (red. - praca zbiorowa), „Testowanie i projektowanie łatwo testowalnych układów i pakietów cyfrowych, część 1 i 2”. Skrypty Politechniki Śląskiej odpowiednio o nr 1586 i 1788 (in Polish).

Hławiczka A. (red. - praca zbiorowa), „Łatwo testowalne układy i pakiety cyfrowe - projektowanie i testowanie, Wyd. WNT, Warszawa, 1993 (in Polish)

Learning outcomes:

* Knowledge: knows and understands

1. Basic techniques of testing combinational and sequential circuits (laboratory report, final test) K2A_W01; K2A_W02
2. Principles of operation of a scan path and a boundary scan path (laboratory report, final test) K2A_W05
3. Basic concepts about built-in self-test and fault tolerance in digital systems (laboratory report, final test) K2A_W05.

*Skills: is able / can
4. Find a test pattern set or a test sequence and use it to test a simple digital circuit (laboratory report, final test) K2A_U08
5. Use a boundary scan to test a simple digital circuit (laboratory report) K2A_U05; K2A_U08
6. Design and implement a simple BIST structure (laboratory report) K2A_U05; K2A_U08
7. Design and implement a simple fault-tolerant digital circuit (laboratory report) K2A_U05; K2A_U08

Assessment methods and assessment criteria:

1. The condition for obtaining a credit in the Design for testability subject is:
a. obtaining a positive grade for all laboratory classes,
b. obtaining a positive grade for the final test.

2. The course manager, taking into account the results obtained by students in laboratory classes, may release selected or all students from the obligation to write a final test.

3. In the case of students who were released from the obligation to write a final test, the grade obtained from the laboratory is also the final grade for the entire subject.

4. The final laboratory grade is determined on the basis of the weighted average of the grades obtained for each laboratory class.

Making up missed laboratory work is possible on the dates specified in the schedule.

The syllabus is valid from academic year 2022/23 and its content cannot be changed during the semester.

Course credits in various terms:

<without a specific program>

Type of credits	Number	First term	Last term
European Credit Transfer System (ECTS)	3	2022/2023-L	