SYLLABUS

Name: ***Digital circuits (AESAu-A>SI4DC24)***
Name in Polish:
Name in English: ***Digital circuits***

Information on course:

Course offered by department: Faculty of Automatic Control, Electronics and Computer Science
Course for department: Silesian University of Technology

Default type of course examination report:

ZAL

Language:

English

Course homepage:

https://platforma.polsl.pl/rau3/course/view.php?id=80222

Short description:

The course is a part of specialised curriculum content and covers problems of digital systems design from idea to final implementation. The main goals of the subject are hardware components' structure and properties, methods of implementing and properties of elementary functional blocks, design methodologies and tools.

Description:

ECTS: 5
Total workload: 125h (65 contact hours / 60 student's own work hours)
- Lecture: 30h
- Classes: 15h
- Laboratory: 15h
- Tests, revisions, reports defence, discussions: 5h

Student's self work:
- lecture and classes revision tasks
- preparation for laboratories and tests
- self case studies and examples analysis
- writing reports

Lecture:
Basic information about digital signals: quantisation and coding, binary codes, binary coded decimal numbers (BCD), fixed point positive and negative numbers, and symbolic data representation.
General description of digital integrated circuits: scale of integration, digital circuits families Introduction to implementation of logic components in different technologies: RTL (Resistor-Transistor-Logic), TTL (Transistor-Transistor-Logic), MOS transistor and implementation of PMOS/NMOS/CMOS logic components an overview.
CMOS technology: short overview of manufacturing. CMOS components. Implementation of: NAND, NOR, AOI, transmission gate, flip-flops, and multiplexers.
Introduction to Verilog HDL: Difference between program (sequential algorithm) and a description of the parallel system (digital system). Hierarchical description methodology. Methods of describing combinational and sequential blocks. All following issues are illustrated with synthesizable patterns of HDL code.
Combinational circuits implementation: Theory and implementation with use of multiplexers, decoders and lookup tables. Basics of function minimization and decomposition: Minimal primes generation Quinee-McCluskey algorithm, minimal cover problem - Patrick's algorithm, Improving runtime, Espressso algorithm, Shannon expansion and BDD outline, technology mapping for MUX and LUT, Ashenhurst-Curtis decomposition theorem, technology mapping for LUT and PAL
Sequential circuits: Basic flip-flip types (D, T, JK), dynamic properties, building excitation functions for respective flip-flop types.
Counters: asynchronous counters, synchronous counters, basics of operation and synthesis, assessment of maximal clock frequency, control units with counters, hazards in counters, synthesis of counter units.
Shift registers: shifting and loading data structures, counting registers: ring counters, Johnson, LFSRs, properties and applications design of custom counting register, application in counting, data form conversion, diagnostics, data integrity check
Arithmetic circuits: Fundamentals of natural and signed number representation and operations, complement numeral systems. adder – the ripple carry adder, design, properties assessment, carry look ahead adder - design and implementation, BCD adder,Multipliers – combinational implementation, sequential implementation, mixed approach, pipe lining. Conversion between BCD (or other custom radix) and Binary representation parallel and serial implementations.
Control unit design: Introduction to microprogrammable circuits as systematic method of control unit design, methods of reducing ROM size and its influence on unit architecture, developing an equivalent graph and its limitations.
Programmable Logic Devices: Elementary architectures PLE, PLA, PAL, CPLD architecture, FPGA architecture, general information, resources, CLB architecture, LUT, carry chain, clock signal distribution and synthesis (DLL/PLL), dedicated hardware cores (memory, DSP blocks, processing units) Implementing FSMs with use of programmable logic devices, PLA, PLE and PAL circuits, examples. Methods of decomposition of FSM
Memories: architecture, implementation, SRAM, DRAM, SDRAM, memories-based components: stacks (LIFO) and queues (FIFO), memories expansion of word and capacity
Data input-output devices: key, matrix keyboards, interfacing, debouncing methods, LED, 7-segment displays in LED and LCD, display control methodology static and multiplexed.
Data transmission: Structure of digital systems, asynchronous serial and parallel transmission, handshaking, bus protocol, transmission lines in digital systems.
Analog to digital converters: signal conversion method: flash, successive approximation, double integration, conversion errors, accuracy, noise dumping
Digital to analog converters: basic structures, conversion accuracy and error definitions

Classes:

1. Logic components: architecture and electrical properties, equivalent linear models, driving indicators, relays, and other loads, interaction with passive components resistors and capacitors, calculating of threshold voltages, time dependencies, transient analysis, generators.
2. Logic functions implementation and decomposition with use of multiplexer, decoders, and lookup tables (basics of FPGA architecture).
3. Register and counters: architectures, shift registers, shift-parallel registers, designing custom counters and registers, counting register, cycle self-adjustment, dynamic properties.
4. Arithmetic circuits – basic of arithmetic circuits, adder, addition and subtraction units for two's and one's complement system, multipliers, code converters (BCD – BIN) parallel and serial.
5. Microprogrammable logic circuits, architecture, graph transformations, implementation, interacting with counters, sequential dependencies between machines.
6. Designing digital circuits with programmable logic components CPLD and FPGA.

Laboratory:
Practical verification of presented problems covering the following issues:
1. Static and dynamic characteristics of gates
2. Arithmetic circuits
3. Memory blocks, stacks, queues
4. Microprogrammable logic circuits
5. Digital frequency meter
6. Analog to digital converters, digital to analog converters

Bibliography:

1. C. Morris Mano, C.R. Kim: Logic and Computer Design Fundamental. Pearson ISBN-13: 978-0133760637
2. C.H. Roth, L.L. Kinney, E.B. John Cengage Fundamentals of Logic Design ISBN-13: 978-1337620352
3. S. Palnitkar: Verilog HDL - A Guide to Digital Design and Synthesis. Sunsoft Press ISBN-13: 978-0132599702
4. J.D. Daniels: Digital Design from Zero to One. John Wiley & Sons, 1996
5. J.P. Hayes: Digital Logic Design. Addison Wesley, 1993

Learning outcomes:

1. Has knowledge of principles of implementation and operation of digital circuits. Has knowledge of design methodologies of digital systems implemented in basic technologies including programmable technologies (CPLD, FPGA). (K1A_W8)
2. Has knowledge of operation and design of combinational logic circuits, sequential and microprogrammable circuits. (K1A_W9)
3. Has knowledge and understood methodologies of designing digital circuits including control systems. Is able to use CAD/CAE software in design and verification process.(K1A_W12)
4. Is able to use computer aided design and engineering tools (CAD/CAE) in design and implementation process of digital systems. (K1A_U4)
5. Is able to work independently and in team. Is able to cooperate with other team members.(K1A_U5)
6. Is able to design and implement digital systems (K1A_U13)-
7. Understands the necessity of continues learning. Is aware of knowledge significance in solving problems.(K1A_K1)

Assessment methods and assessment criteria:

Students need to pass written tests from practice (P) and theory (T). The practical test consists of 3 tasks. The theoretical test consists from 6 questions (typically). On both tests, students must obtain a minimum of 50% to pass.
All laboratory exercises must be completed and all reports must be delivered and accepted. Final laboratory grade (L) is calculated as average of all grades consisting of laboratory activity and report.
The final grade is calculated as: Grade = (P + T + L)/3

The grade is rounded according to the following rules:

3.00 - 3.29	3.0
3.30 - 3.79	3.5
3.80 – 4.29	4.0
4.30 - 4.64	4.5
4.65 - 5.00	5.0

The syllabus is valid from academic year 2025/2026 and its content cannot be changed during the semester.

Course credits in various terms:

<without a specific program>

Type of credits	Number	First term	Last term
European Credit Transfer System (ECTS)	5	2024/2025-Z	