SYLLABUS

Name: ***Hardware description languages (VHDL/Verilog) (AESAu-E>SI7M-HDL24)***
Name in Polish:
Name in English: ***Hardware desription languages (VHDL/Verilog)***

Information on course:

Course offered by department: Faculty of Automatic Control, Electronics and Computer Science
Course for department: Silesian University of Technology

Default type of course examination report:

ZAL

Language:

English

Course homepage:

https://platforma.polsl.pl/rau3/course/view.php?id=80579

Short description:

The course aims to familiarise students with designing digital circuits using the Verilog HDL and/or VHDL (hardware description language).

The course participant should have a background in the theory of logic circuits, digital circuits design and microprocessor design.

Description:

ECTS: 3
Total workload: 125 hours (65 contact hours, 60 students' own work hours)
Forms of contact hours:
Lecture 30h
Laboratory 30h
Other (e.g. reports revision and discussion) 5h

Students' own work: preparation for lab classes, writing reports

Lecture
1. Designing complex digital circuits
2. Basic features of hardware description languages
3. The most important lexical structures of VHDL and Verilog HDL
4a. VHDL synthesizable subset
4b. Synthesizable constructs in Verilog HDL
5. Basics of functional verification: writing simple testbenches
6. Modelling basic digital circuits in VHDL and Verilog HDL
7. Verifikation through simulation

Laboratory:
The aim of these classes is to familiarise students with the Verilog HDL and VHDL, and how they are applied in the design of complex digital circuits. The classes involve writing simple models, verifying them through simulation, their synthesis and practical testing.
In the remaining exercises, students will design a complex digital circuit.

1. The basics of using software to simulate, synthesise and implement digital circuits.
2. Writing synthesizable models of combinational circuits, including translators, multiplexers, decoders, demultiplexers and arithmetic circuits.
3. Simulation and testing of combinational circuits.
4. Writing synthesizable models of sequential circuits, including asynchronous flip-flops, circuits with latch-type synchronisation mechanisms, edge-triggered circuits, counters, registers and FSMs.
5. Simulation and testing of synchronous circuits.
6. Creating complex hierarchical models.
7. Mixed-mode simulation and synthesis.
8. Designing a complex digital circuit.

Bibliography:

Palnitkar S., Verilog HDL. A Guide to Digital Design and Synthesis, Prentice Hall, 2003
Lee W.F., Verilog Coding for Logic Synthesis, John Wiley & Sons Inc., 2003
Lee J.M., Verilog Quickstart: A Practical Guide to Simulation and Synthesis in Verilog, Kluwer Academic Publishers, 2002
Bhasker J., Verilog HDL Synthesis. A practical Primer, Star Galaxy Publishing, 1998
Doulos, The Verilog Golden Reference Guide, Doulos, 1996

Gazi O., A Tutorial Introduction to VHDL Programming, Springer, 2019
Perry D., VHDL: Programming by Example, 4th Ed., McGraw Hill Education, 2017
Brown S., Vranesic Z., Fundamentals of Digital Logic with VHDL Design, 3rd Ed. McGraw Hill Education, 2017
Bhasker J., A VHDL Primer, 3rd Ed., Pearson, 2015
Ashenden P. J.: Student's Guide to VHDL, Morgan Kaufmann Publishers Inc., 2008, ISBN: 978-1-55860-865-8

Mano M., Ciletti M. D., Digital Design. With an Introduction to the Verilog HDL, VHDL, and System Verilog, Pearson Education Limited, 2019

Learning outcomes:

Course-specific learning outcomes

At the completion of the course, student:
1. Knows and understands the methodology of designing digital circuits (including integrated circuits) and digital systems (test, laboratory

report, project) K1A_W8; K1A_W9
2. Knows and understands hardware description languages and computer tools for designing and simulating circuits and systems (test, laboratory report, project) K1A_W11
3. Is able to formulate the specification of a digital system at the level of implemented functions, also using hardware description languages (test, laboratory report, project) K1A_U1; K1A_U3; KA1_U6
4. Is able to design simple digital circuits and systems (test, laboratory report, project) K1A_U4
5. Is able to critically analyze and evaluate the operation and properties of a designed digital circuit or system (test, laboratory report, project) K1A_U3; K1A_K1
6. Is ready to make the necessary modifications to the designed layout or system in order to improve its operation and/or parameters (test, laboratory report, project) K1A_U4; K1A_U6; K1A_K1
7. Is able work individually and in a team; is able to estimate the time needed to complete a task (observation of student activity and skills) K1A_U3; K1A_U5

Assessment methods and assessment criteria:

HDL Course consists of two components: lecture and laboratory. According to SUT regulation, lecture attendance is optional (however highly recommended), whereas laboratory exercises are obligatory.

The laboratory exercises are carried out by two or three people in each section. Students have to complete all exercises and prepare reports (one per section). The report should include elements specified by the teacher.
If for some reason the labs are done remotely, all students must do the remote labs, but a report must be prepared one per section. Each report should be completed within one weeks period. Reports should be prepared in the electronic form; declaration of student's original work is necessary in this case. Teachers
may verify obtained results.

Making up missed laboratory work is possible on the dates specified in the schedule

Lecture and lab assessments are carried out in the form of written and/or practical tests.

The syllabus is valid from academic year 2024/25 and its content cannot be changed during the semester.

Course credits in various terms:

<without a specific program>

Type of credits	Number	First term	Last term
European Credit Transfer System (ECTS)	3	2024/2025-Z	